16 Bit 4LSB Vout *nano*Dac™, Buffered, 3V/5V, Sot 23

Preliminary Technical Data

AD5061

FEATURES

- Single 16-Bit DAC, 4 Lsb inl.
- 1.8 Volt Digital Interface Capability
- Power-On-Reset to Zero Volts/Mid Scale
- Three Power-Down Functions
- Low Power Serial Interface with Schmitt-Triggered Inputs
- 8-Lead Sot23
- Low Power Operation
- Fast Settling.
- Low Glitch on Powerup.

APPLICATIONS

- Process Control
- Data Acquisition Systems
- Portable Battery Powered Instruments
- Digital Gain and Offset Adjustment
- Programmable Voltage and Current Sources
- Programmable Attenuators

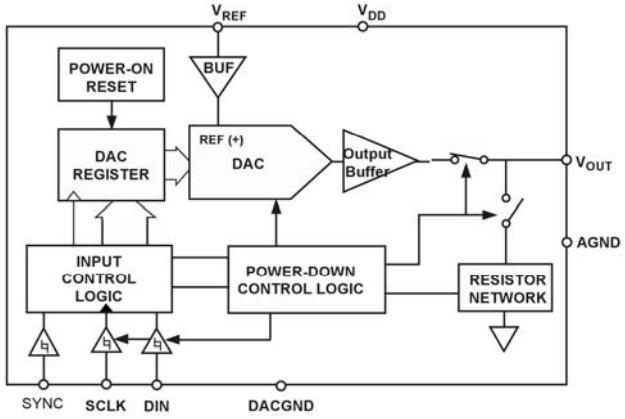
GENERAL DESCRIPTION

The AD5061, a member of the *nano*DAC™ family, is a single 16-bit buffered voltage out DAC, available in a 8 ld Sot23. The AD5061 can be operated at 3V/5V.

The part utilizes a versatile three-wire serial interface that operates at clock rates up to 30 MHz and is compatible with standard SPI™, QSPI™, MICROWIRE™ and DSP interface standards.

The reference for the AD5061 is supplied from an external REF pin. A reference buffer is also provided on chip. The parts incorporate a power-on-reset circuit that ensures that the DAC output powers up to zero volts/ mid scale and remains there until a valid write takes place to the device. The parts also contain a power-down feature that reduces the current consumption of the device to 50nA at 5 V and provides software selectable output loads while in power-down mode. The part is put into power-down mode over the serial interface. Total unadjusted error for the part is <1mV.

These parts also provide a very low glitch on power-up.



AD5061

Part Number	Description
AD5062	2.7 V to 5.5 V, 16 Bit ***nano*DAC™** D/A, 1LSBs INL., Unbuffered, Sot 23.
AD5063	2.7 V to 5.5 V, 16 Bit ***nano*DAC™** D/A, 1 LSBs INL., Unbuffered, 10 uSOIC, uncommitted bi-polar resistors.
AD5040/60	2.7 V to 5.5 V, 14/16 Bit ***nano*DAC™** D/A, 1 LSBs INL, Buffered, Sot23.

PRODUCT HIGHLIGHTS

1. Available in 8-lead SOT23.
2. 16 Bit Accurate, 4 LSB INL.
3. Low Glitch on Power-up.
4. High speed serial interface with clock speeds up to 30 MHz.
5. Three power down modes available to the user.

Rev. PrC

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AD5061—SPECIFICATIONS[1]

AD5061, V_{DD} = 5.5V, Vref =4.096V, RL=5k, 200pF . T_{MIN} to T_{MAX}; unless otherwise noted.

Parameter	B Version[1] Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					
AD5061					
Resolution	16			Bits	
Relative Accuracy			±4	LSB	
TUE		0.5		mV	
Differential Nonlinearity			±1	LSB	Guaranteed Monotonic by Design.
Offset Error		+/-0.125		% of FSR	
Zero Code Error		+/-0.2		mv	Code 160 loaded to dac reg
Full scale Error		+/-0.01		LSB	All 1's loaded to dac reg
Gain Error		+/-0.04		% of FSR	
Offset Drift		6		µV/°C	
Gain Temperature Coefficient		2.5		ppm of FSR/°C	
OUTPUT CHARACTERISTICS					
Output Voltage Range	0		V_{ref} -150mV	V	
Output Voltage Settling Time		10		µs	1/4 to 3/4 to +/-1lsb
Slew Rate		1		V/µs	
Capacitive Load Stability		470		pF	RL=
		1000		pF	RL = 5K
Output Noise Spectral Density		50		nV/√Hz	DAC code=TBD , 1kHz
		50		nV/√Hz	DAC code=TBD , 10kHz
Digital-to-Analog Glitch Impulse		5		nV-s	1 LSB Change Around Major Carry.
Digital Feedthrough		0.5		nV-s	
DC Output Impedance		1		Ω	
REFERENCE INPUT/OUPUT					
Vref Input Range	2		$V_{DD-100mV}$	V	
Input Current		1		uA	
DC Input Impedance	1			MΩ	
LOGIC INPUTS					
Input Current			±1	µA	
V_{INL}, Input Low Voltage	0.8			V	V_{DD} = +5 V
V_{INH}, Input High Voltage			1.8	V	V_{DD} = +5 V
V_{INL}, Input Low Voltage	0.6			V	V_{DD} = +3 V
V_{INH}, Input High Voltage			1.4	V	V_{DD} = +3 V
Pin Capacitance	3			pF	
POWER REQUIREMENTS					
V_{DD}	2.7		3.6	V	AD5060 (3 Volt Option)
I_{DD} (Normal Mode)					DAC Active and Excluding Load Current
V_{DD} = +2.7 V to +3.6 V		900		µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
I_{DD} (All Power-Down Modes)					
V_{DD}	5.0		5.5	V	AD5060 (5 Volt Option)
I_{DD} (Normal Mode)					DAC Active and Excluding Load Current

Parameter	B Version[1] Min	Typ	Max	Unit	Test Conditions/Comments
V_{DD} = +5.0 V to +5.5 V I_{DD} (All Power-Down Modes)		1.3		mA	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} I_{DD} (Normal Mode) V_{DD} = +2.7 V to +5.5 V	2.7		5.5	V	AD5040 DAC Active and Excluding Load Current
I_{DD} (All Power-Down Modes)		50		nA	$V_{IH} = V_{DD}$ and V_{IL} = GND
PSSR		0.5		LSB	VDD +/- 10%

NOTES

[1]Temperature ranges are as follows: B Version: –40°C to +125°C, typical at 25°C.

[2]Guaranteed by design and characterization, not production tested.

3 Linearity calculated using a reduced code range 480-64716.

Specifications subject to change without notice.

TIMING CHARACTERISTICS

(V_{DD} = 2.7-5.5 V; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Limit[1]		Unit	Test Conditions/Comments
t_1[3]	33		ns min	SCLK Cycle Time
t_2	13		ns min	SCLK High Time
t_3	12		ns min	SCLK Low Time
t_4	13		ns min	SYNC to SCLK Falling Edge Setup Time
t_5	5		ns min	Data Setup Time
t_6	4.5		ns min	Data Hold Time
t_7	0		ns min	SCLK Falling Edge to SYNC Rising Edge
t_8	33		ns min	Minimum SYNC High Time
t_9	13		ns min	SYNC Rising Edge to next SCLK Fall Ignore

.

NOTES

[1]All input signals are specified with tr = tf = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.

[2]See Figure 1.

[3]Maximum SCLK frequency is 30 MHz.

Specifications subject to change without notice.

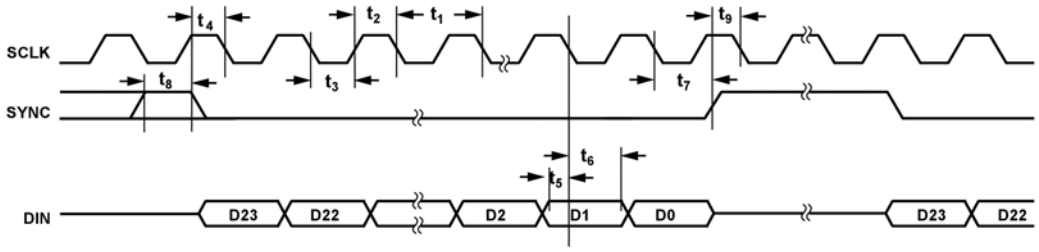


Figure 1. Timing DiagramAD506. AD5040 has same timing specs with 14 bit Word.

ABSOLUTE MAXIMUM RATINGS

Table 1. Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

Parameter	Rating
V_{DD} to GND	–0.3 V to + 7.0 V
Digital Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND[1]	–0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Maximum Junction Temperature	150°C
SOT23 Package	
Power Dissipation	(Tj Max-Ta)/ θ_{JA}
θ_{JA} Thermal Impedance	229.6°C/W
θ_{JC} Thermal Impedance	91.99°C/W
Lead Temperature, Soldering	
Vapour Phase (60 Sec)	300°C
Infrared (15 Sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

Model	Temperature Range	INL	Description	Package Options
AD5061BRJ-1	-40°C to 125 °C	4 LSB	5V, Buffered DAC in SOT-23, Reset to Zero	RT8
AD5061BRJ-2	-40°C to 125 °C	4 LSB	5V, Buffered DAC in SOT-23, Reset to Mid	RT8
AD5061BRJ-3	-40°C to 125 °C	4 LSB	3V, Buffered DAC in SOT-23, Reset to Zero	RT8

PIN CONFIGURATION AND FUNCTION DESCRIPTION

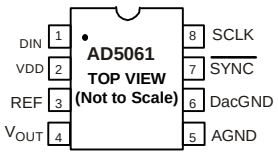


Figure 2. AD5062 8 ld SOT23

Table 2. Pin Function Descriptions

Mnemonic	Function
V_{DD}	Power Supply Input. These parts can be operated from +2.5 V to +5.5 V and V_{DD} should be decoupled to GND.
REF	Reference Voltage Input.
DacGND	Ground input to the DAC.
V_{OUT}	Analog output voltage from DAC.
SYNC	Level triggered control input (active low). This is the frame synchronization signal for the input data. When SYNC goes low, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 16th clock cycle unless SYNC is taken high before this edge in which case the rising edge of SYNC acts as an interrupt and the write sequence is ignored by the DAC.
SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30 MHz.
D_{IN}	Serial Data Input. This device has a 24 bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
AGND	Ground reference point for Analog circuitry on the part.

TERMINOLOGY

Relative Accuracy

For the DAC, relative accuracy or Integral Nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 2.

Differential Nonlinearity

Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 3.

Zero-Code Error

Zero-code error is a measure of the output error when zero code (0000Hex) is loaded to the DAC register. Ideally the output should be 0 V. The zero-code error is always positive in the AD5061 because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in mV. A plot of zero-code error vs. temperature can be seen in Figure 6.

Full-Scale Error

Full-scale error is a measure of the output error when full-scale code (FFFF Hex) is loaded to the DAC register. Ideally the output should be V_{DD} – 1 LSB. Full-scale error is expressed in percent of full-scale range. A plot of full-scale error vs. temperature can be seen in Figure 6.

Gain Error

This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percent of the full-scale range.

Total Unadjusted Error

Total Unadjusted Error (TUE) is a measure of the output error taking all the various errors into account. A typical TUE vs. code plot can be seen in Figure 4.

Zero-Code Error Drift

This is a measure of the change in zero-code error with a change in temperature. It is expressed in µV/°C.

Gain Error Drift

This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV secs and is measured when the digital input code is changed by
1 LSB at the major carry transition (7FFF Hex to 8000 Hex). See Figure 19.

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC but is measured when the DAC output is not updated. It is specified in nV secs and measured with a full-scale code change on the data bus, i.e., from all 0s to all 1s and vice versa.

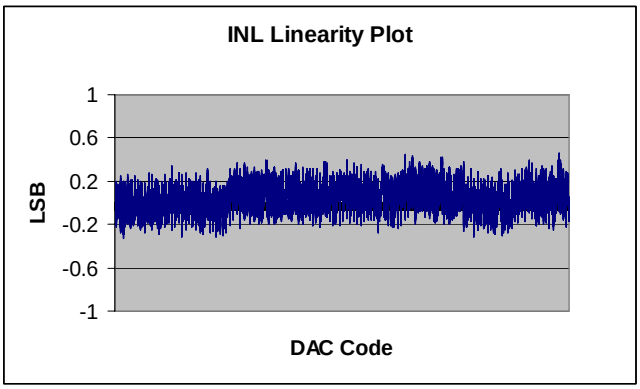


Figure 3. Typical INL Plot

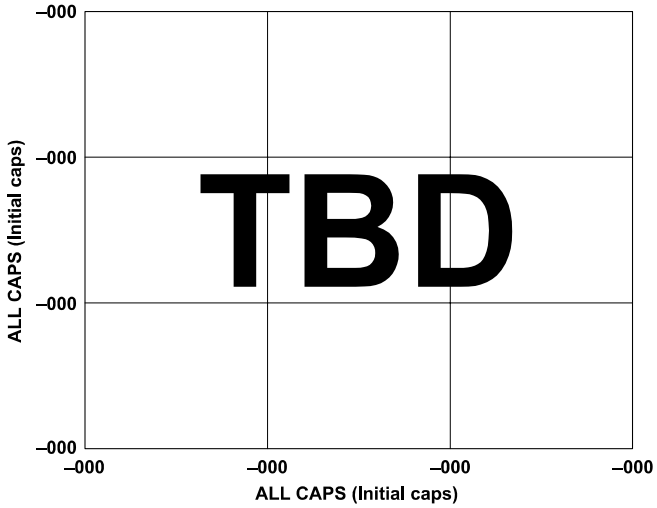


Figure 4. Total Unadjusted Error Polt.

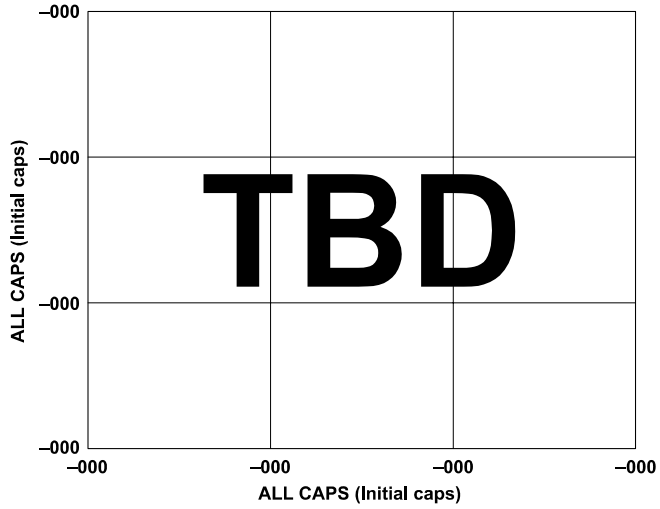


Figure 5. Zero Scale Error and Full Scale Error vs. Temperature

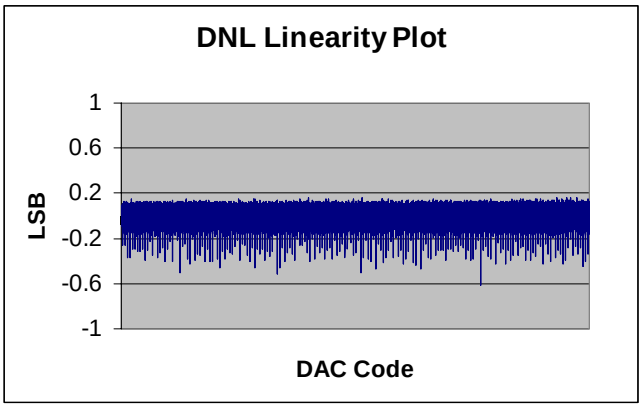


Figure 6. Typical DNL PloT.

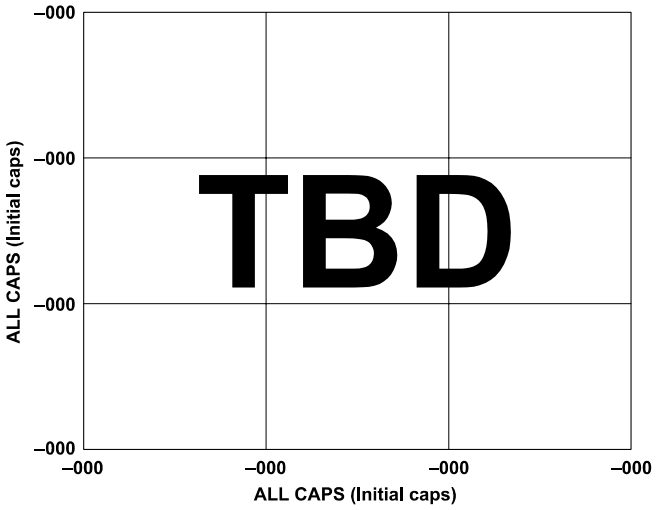


Figure 7. INL & DNLvs Supply

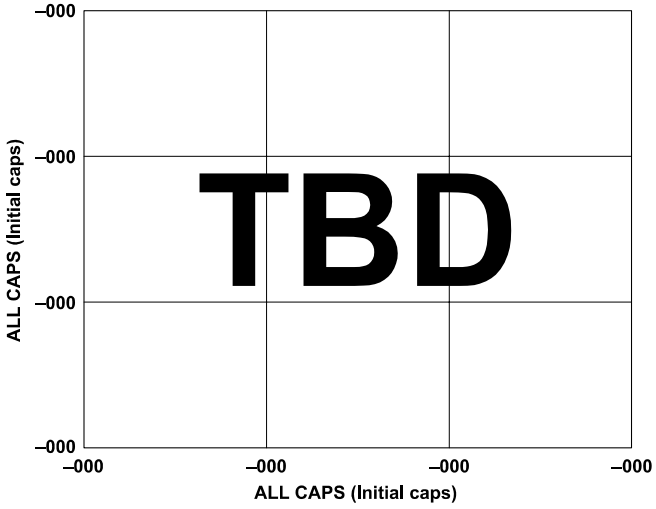


Figure 8. Idd Histogram @ Vdd=3/5 Volts.

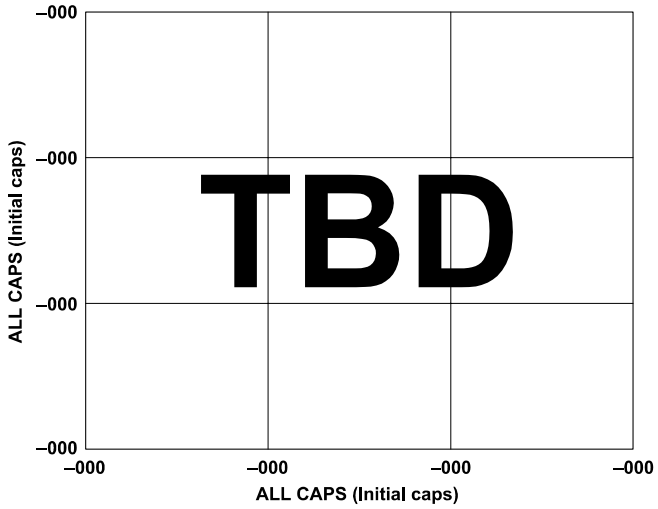


Figure 9. Source and Sink Current Capability

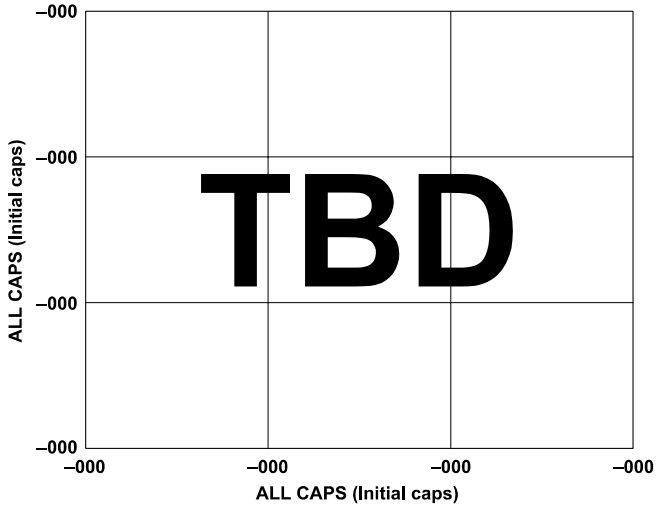


Figure 10. Supply Current vs. Temperature

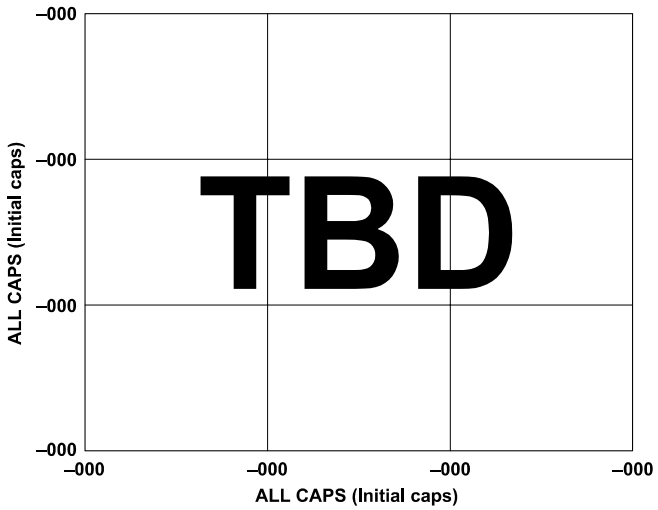


Figure 11. Full Scale Settling Time

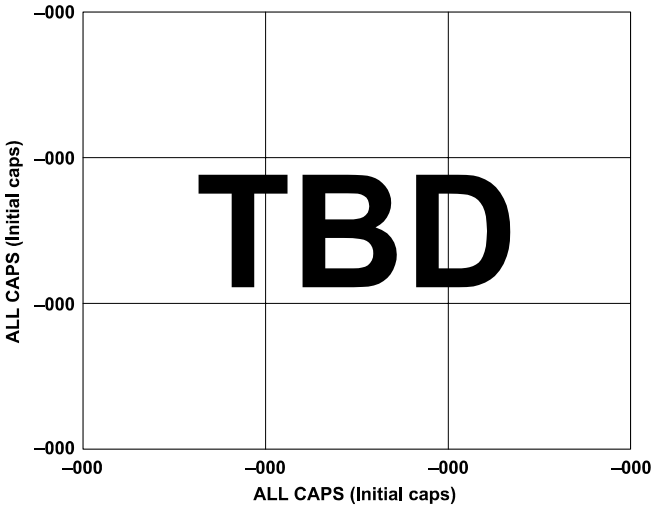


Figure 12. Supply Current vs Code.

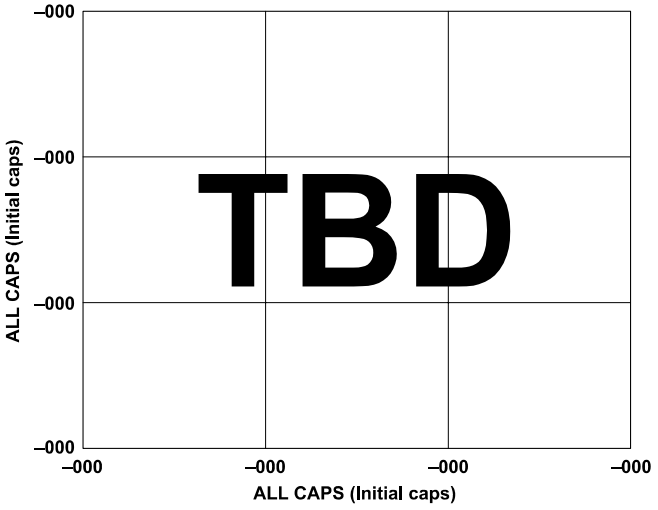


Figure 13. Supply Current vs SupplyoVoltage

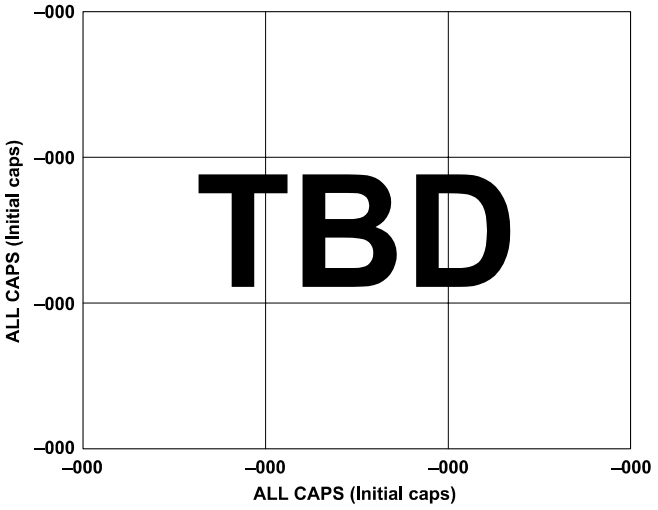


Figure 14. Half Scale Settling Time

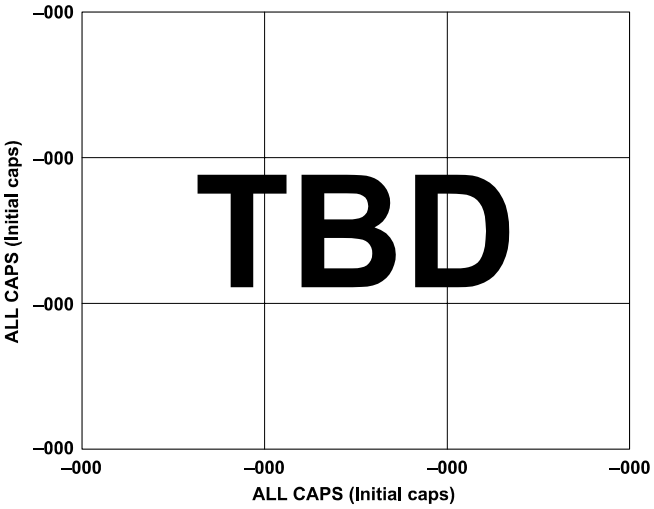


Figure 15. Power on Reset to 0 Volts.

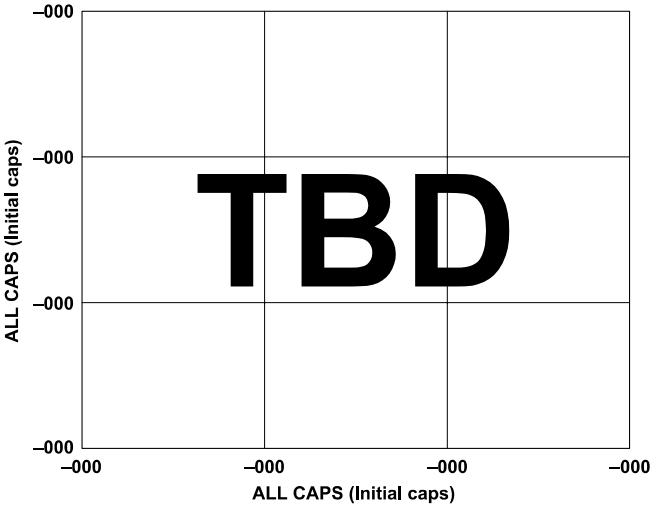


Figure 16. Digital to Analog Glitch Impulse

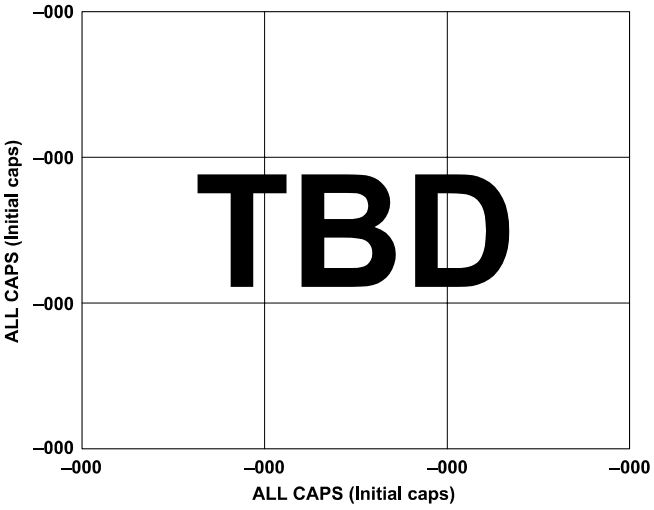


Figure 17. Output Spectral Density 100k Bandwidth

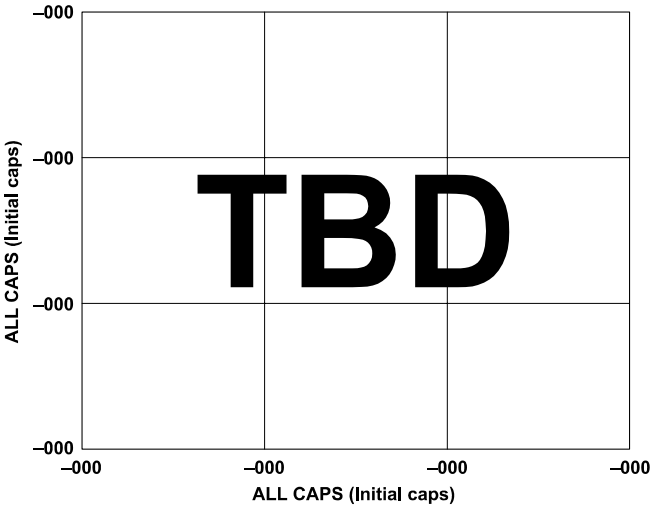


Figure 18. Exiting Power-Down

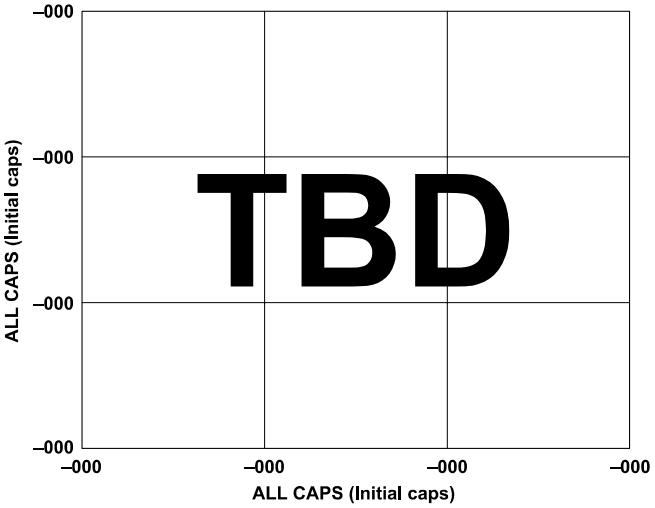


Figure 19. Harmonic Distortion on igitally Generated Waveform.

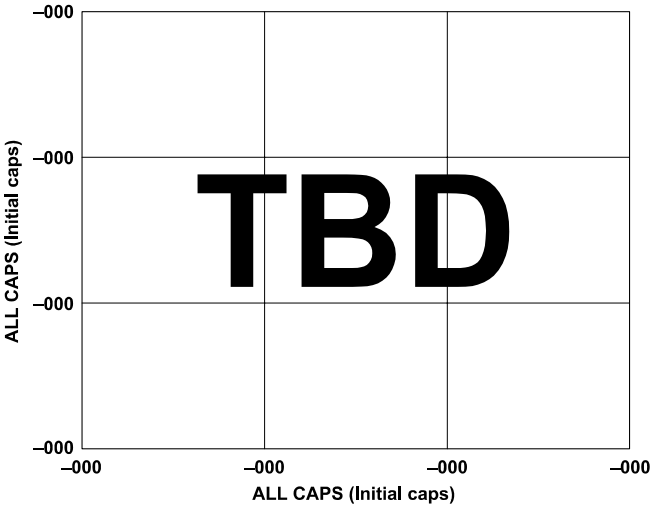


Figure 20. 0.1 Hz to 10 Hz Noise Plot

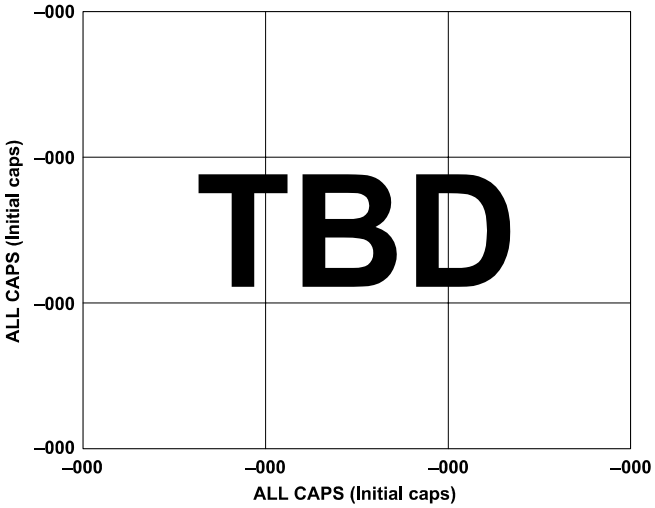


Figure 21. PowerUp Transient

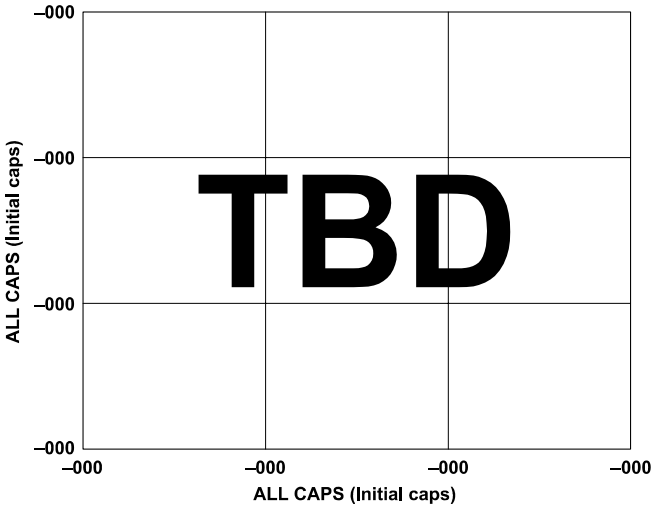


Figure 22. Glitch Energy

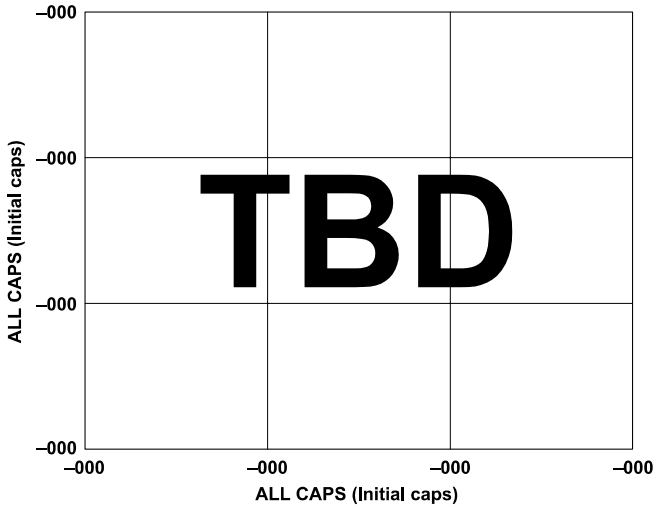


Figure 23. Offset Error Distribution

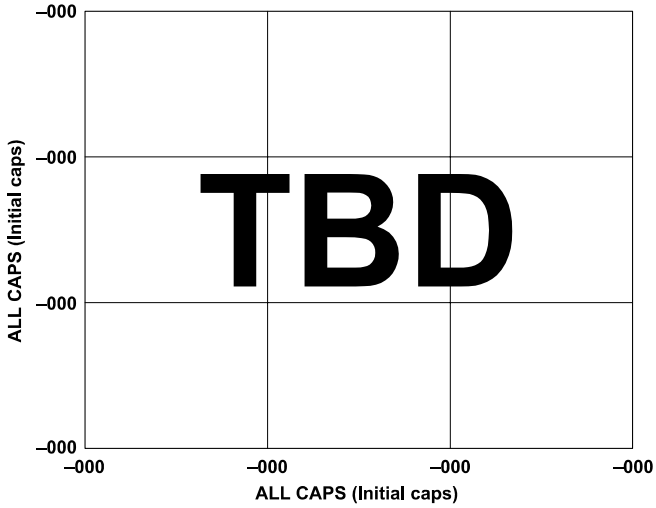


Figure 24. Gain Error Distribution

GENERAL DESCRIPTION

The AD5061 is a single 16-bit, serial input, voltage output DACs. The AD5061 operates from either a 3V or 5V supply. Data is written to the AD50461in a 24-bit word format.

The AD5061 incorporates a power-on reset circuit, which ensures that the DAC output powers up to 0 V or mid-scale. The device also has a software power-down mode pin, which reduces the typical current consumption to 50nA at 3V.

DAC Architecture

The DAC architecture of the AD5061 consists of two matched DAC sections. A simplifed circuit diagram is shown in Figure X The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either AGND or VREF. The remaining 12 bits of thedata word drive switches S0 to S11 of a 12-bit voltage modeR-2R ladder network.

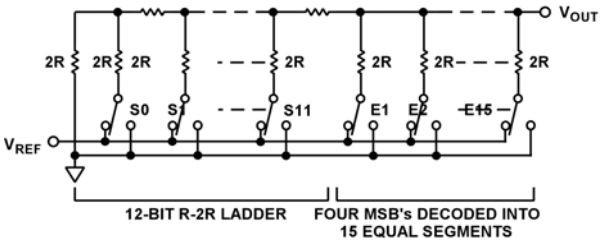


Figure X. DAC Ladder Structure

Reference Buffer

The AD5061 operates with an external reference. The reference input (REFIN) has an input range of up to Vdd. This input voltage is then used to provide a buffered reference for the DAC core

SERIAL INTERFACE

The AD5061 (24 bit word write) has a three-wire serial interface (SYNC, SCLK and DIN), which is compatible with SPI, QSPI and MICROWIRE interface standards as well as most DSPs. See Figure 1 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the SYNC line low. Data from the DIN line is clocked into the 24-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making these parts compatible with high speed DSPs. On the 24th falling clock edge, the last data bit is clocked in and the programmed function is executed (i.e., a change in DAC register contents and/or a change in the mode of operation). At this stage, the SYNC line may be kept low or be brought high. In either case, it must be brought high for a minimum of 33 ns before the next write sequence so that a falling edge of SYNC can initiate the next write sequence. Since the SYNC buffer draws more current when V_{IN} = 1.8 V than it does when V_{IN} = 0.8 V, SYNC should be idled low between write sequences for even lower power operation of the part. As is mentioned above, however, it must be brought high again just before the next write sequence.

Input Shift Register

The input shift register is 24 bits wide (see Figure 22/23). D23-D16 are set to zero for normal operation. D17, D16 are control bits that control which mode of operation the part is in (normal mode or any one of three power-down modes). There is a more complete description of the various modes in the Power-Down Modes section. The next sixteen bits are the data bits. These are transferred to the DAC register on the 24th falling edge of SCLK.

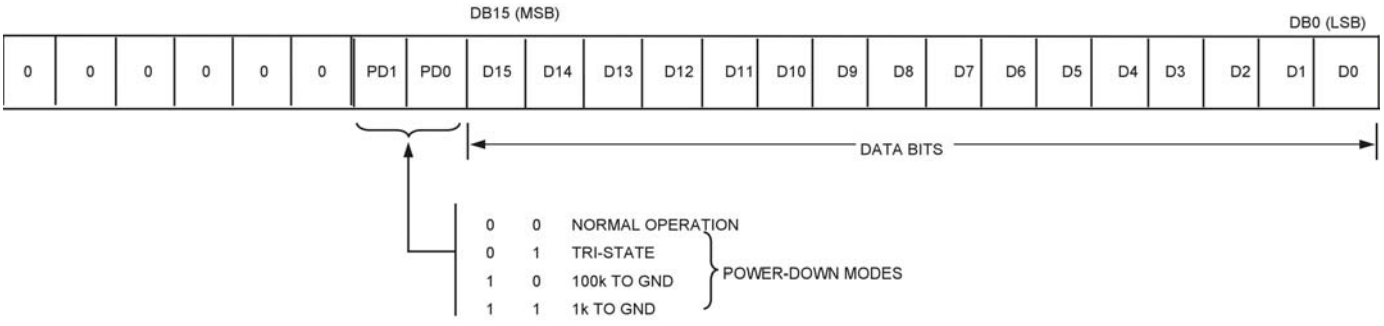


Figure 22. AD5060 Input Register Contents

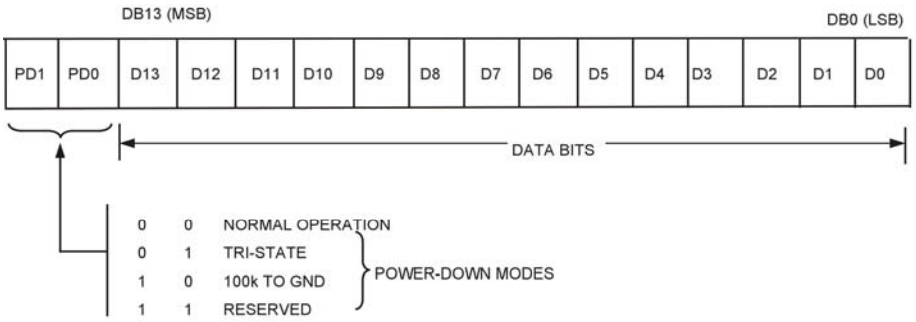


Figure 22. AD5040 Input Register Contents

SYNC Interrupt

In normal write sequence, the SYNC line is kept low for at least 24 falling edges of SCLK and the DAC is updated on the 24th falling edge. However, if SYNC is brought high before the 24th falling edge this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents or a change in the operating mode occurs—see Figure 23.

Power-On-Reset

The AD5061 contains a power-on-reset circuit that controls the output voltage during power-up. The DAC register is filled with zeros and the output voltage is zero volts/mid-scale. It remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

Software Reset.

The AD5061 can be put into software reset by setting all in the Dac register to one. This includes writing ones to bits D23-D16, which in not the normal mode of operation. **Note: The SYNC Interrupt command cannot be performed if a software reset command is started.**

Power-Down Modes

The AD5061 contains three separate modes of operation. These modes are software-programmable by setting two bits (PD1 and PD0) in the control register. Table I shows how the state of the bits corresponds to the mode of operation of the device.

Table I. Modes of Operation for the AD5061

PD1	PD0	Operating Mode
0	0	Normal Operation Power-Down Mode
0	1	TRI-STATE
1	0	100 kΩ to GND
1	1	1 kΩ to GND *

When both bits are set to 0, the part works normally with its normal power consumption. However, for the three power-down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current fall but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options. The output is connected internally to GND through a 1kΩ resistor, a 100 kΩ resistor or it is left open-circuited (Three-State). The output stage is illustrated in Figure 24.

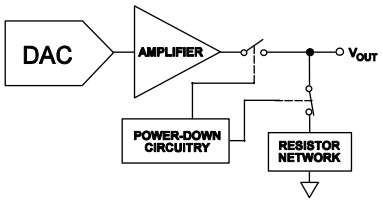


Figure 24. Output Stage During Power-Down

The bias generator, the output amplifier, the DAC and other associated linear circuitry are all shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5 μs for V_{DD} = 5 V and 5 μs for V_{DD} = 3 V. See Figure 18 for a plot.

MICROPROCESSOR INTERFACING

AD5061 to ADSP-2101/ADSP-2103 Interface

Figure 25 shows a serial interface between the AD5061 and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 should be set up to operate in the SPORT Transmit Alternate Framing Mode. The ADSP-2101/ADSP-2103 SPORT is programmed through the SPORT control register and should be configured as follows: Internal Clock Operation, Active Low Framing, 16-Bit Word Length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled.

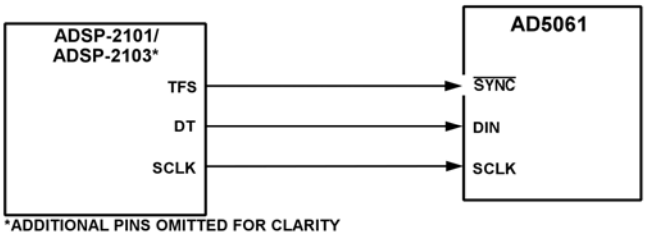


Figure 25. AD5061 to ADSP-2101/ADSP-2103 Interface

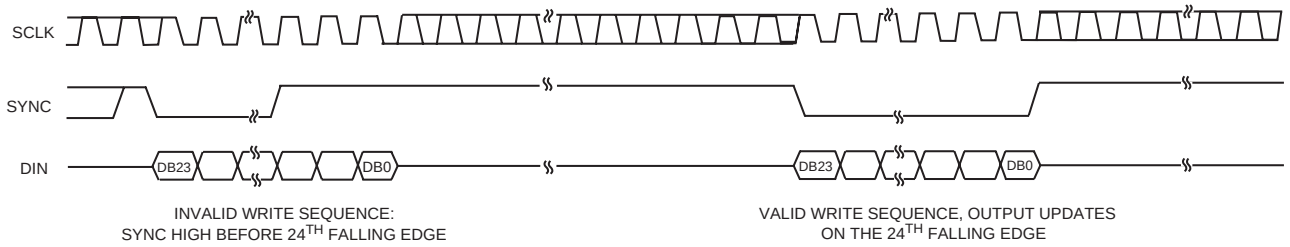


Figure 23. SYNC Interrupt Facility for AD5060.

AD5061 to 68HC11/68L11 Interface

Figure 26 shows a serial interface between the AD5060 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5060, while the MOSI output drives the serial data line of the DAC. The SYNC signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are as follows: the 68HC11/68L11 should be configured so that its CPOL bit is a 0 and its CPHA bit is a 1. When data is being transmitted to the DAC, the SYNC line is taken low (PC7). When the 68HC11/68L11 is configured as above, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to load data to the AD5061, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC and PC7 is taken high at the end of this procedure.

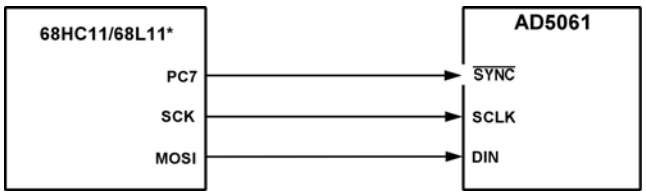


Figure 26. AD5061 to 68HC11/68L11 Interface

AD5061 to Blackfin ADSP-BF53X Interface

Figure 2X shows a serial interface between the AD5641 and the Blackfin ADSP-53X microprocessor. The ADSP-BF53X processor family incorporates two dual-channel synchronous serial ports, SPORT1 and SPORT0 for serial and multiprocessor communications. Using SPORT0 to connect to the AD5062/63, the setup for the interface is as follows. DT0PRI drives the SDIN pin of the AD5062/63, while TSCLK0 drives the SCLK of the part. The SYNC is driven from TFS0.

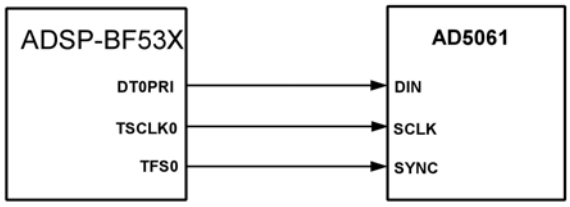


Figure 2X. AD5061 to Blackfin ADSP-BF53X Interface

AD5061 to 80C51/80L51 Interface

Figure 27 shows a serial interface between the AD5061 and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TXD of the 80C51/80L51 drives SCLK of the AD5061, while RXD drives the serial data line of the part. The SYNC signal is again derived from a bit programmable pin on the port. In this case port line P3.3 is used. When data is to be transmitted to the AD5061, P3.3 is taken low. The 80C51/80L51 transmits data only in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low

after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 outputs the serial data in a format which has the LSB first. The AD5061 requires its data with the MSB as the first bit received. The 80C51/80L51 transmit routine should take this into account.

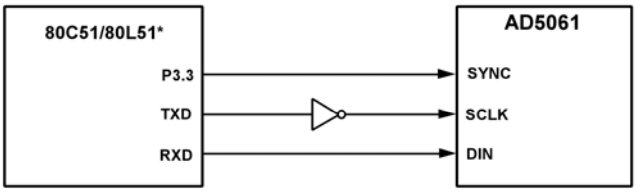


Figure 27. AD5061 to 80C51/80L51 Interface

AD5061 to Microwire Interface

Figure 28 shows an interface between the AD5061 and any microwire compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5061 on the rising edge of the SK.

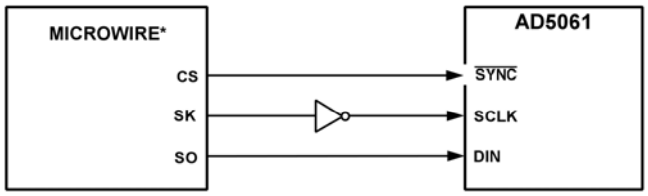


Figure 28. AD5061 to MICROWIRE Interface

APPLICATIONS
Choosing a Reference for the AD5061.

To achieve the optimum performance from the AD5060, thought should be given to the choice of a precision voltage reference. The AD5061 have just one reference input, REFIN. The voltage on the reference input is used to supply the positive input to the Dac . Therefore any error in the reference will be reflected in the Dac.

There are 4 possible sources of error when choosing a voltage reference for high accuracy applications; initial accuracy, ppm drift, long term drift and output voltage noise. Initial accuracy on the output voltage of the Dac will lead to a full scale error in the Dac. To minimize these errors, a reference with high initial accuracy is preferred. Also, choosing a reference with an output trim adjustment, such as the ADR425 allow a system designer to trim system errors out by setting a reference voltage to a voltage other than the nominal. The trim adjustment can also be used at temperature to trim out any error.

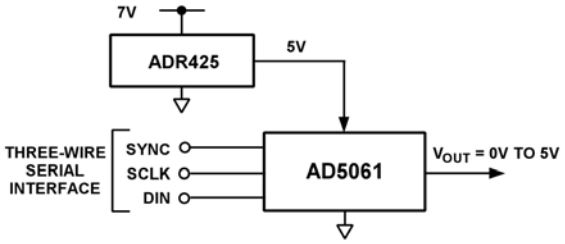


Figure 29. ADR425 as Reference to AD5040. ADR420 can be used for AD5060.

Long term drift is a measure of how much the reference drifts over time. A reference with a tight long term drift specification ensures that the overall solution remains relatively stable during its entire lifetime.

The temperature co-efficient of a references output voltage affect INL,DNL TUE. A reference with a tight temperature co-efficient specification should be chosen to reduce temperatue dependence of the Dac output voltage on ambient conditions.

In high accuracy applications, which have a relatively low noise budget, reference output voltage noise needs to be considered. Choosing a reference with as low an output noise voltage as practical for the system noise resolution required is important. Precision voltage references such as the ADR435 produce low output noise in the 0.1-10Hz region. Examples of some recommended precision references for use as supply to the AD5060 are shown in the figure below..

Part list of precision references for use with AD5061.

Part No.	Initial Accuracy (mV max)	Temp Drift (ppm °C max)	0.1-10Hz Noise (uV p-p typ)
ADR420	+/-6	3	1.75
ADR425	+/-6	3	3.4
ADR02	+/-5	3	15
ADR392	+/-6	25	5

Bipolar Operation Using the AD5061

The AD5061 has been designed for single-supply operation but a bipolar output range is also possible using the circuit in Figure 30. The circuit below will give an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{DD} \times \left(\frac{D}{65536}\right) \times \left(\frac{R1+R2}{R1}\right) - V_{DD} \times \left(\frac{R2}{R1}\right)\right]$$

where *D* represents the input code in decimal (0–65535).
With V_{DD} = 5 V, *R*1 = *R*2 = 10 kW:

$$V_O = \left(\frac{10 \times D}{65536}\right) - 5\,V$$

This is an output voltage range of ±5 V with 0000Hex corresponding to a –5 V output and 3FFF Hex corresponding to a +5 V output.

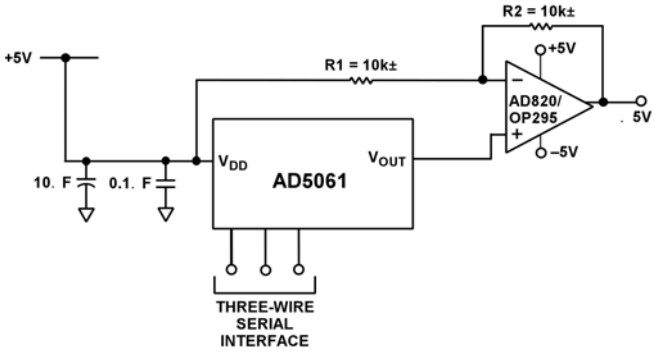


Figure 30. Bipolar Operation with the AD5061

Using AD5061 with an Opto-Isolated Interface Chip.

In process-control applications in industrial environments it is often necessary to use an opto-isolated interface to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur in the area where the DAC is functioning. Because the AD5061 uses a three-wire serial logic interface, the ADuM130Xifamily s an ideal way to provide digital isolation for the DAC interface.

The ADuM130x isolators provide three independent isolation channels in a variety of channel configurations and data rates. They operate across the full range from 2.7V to 5.5V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier.

Figure 31. The power supply to the part also needs to be isolated. This is done by using a transformer. On the DAC side of the transformer, a +5 V regulator provides the +5 V supply required for the AD5061.

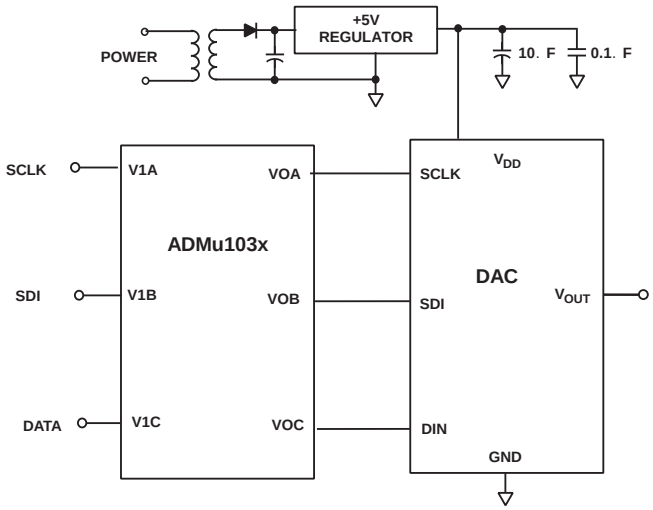


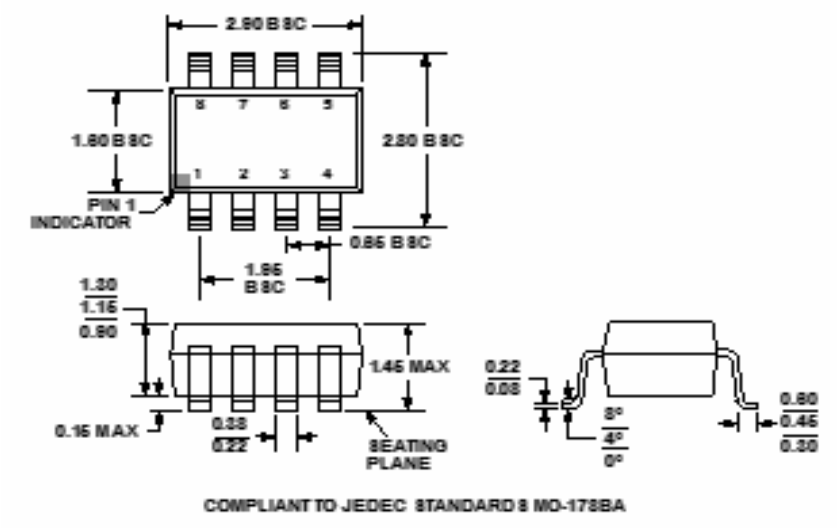
Figure 31. AD5061 with An Opto-Isolated Interface

Power Supply Bypassing and Grounding

When accuracy is important in a circuit it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5061 should have separate analog and digital sections, each having its own area of the board. If the AD5061 is in a system where other devices require an AGND to DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5061.

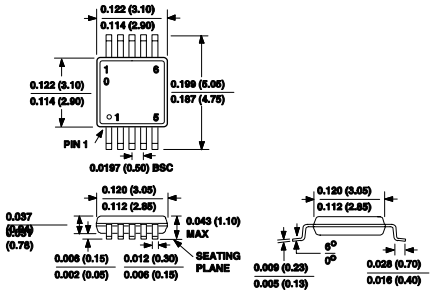
The power supply to the AD5061 should be bypassed with
10 µF and 0.1 µF capacitors. The capacitors should be physically as close as possible to the device with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor has low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), e.g., common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a two-layer board.



8 ld SOT23

Outline Dimensions
Dimensions shown in inches and mms



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